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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,720	01/30/2006	Barend Visser	050588/295500	8410

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EXAMINER

GOODWIN, DAVID J

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/542,720

Applicant(s)

VISSER ET AL.

Examiner

David Goodwin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 July 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 7/20/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 through 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams (US 6,291,298).
3. Williams teaches an insulated gate device comprising a gate connected to a gate terminal (fig 6c) and having a variable input capacitance at the gate terminal (fig 7H) as the device is switched between an off and an on state, a ration between a final value of the capacitance when the device is on and the initial value of the capacitance when the device is off is smaller then 2.0 (column 4 lines 60-67).
4. The power MOSFET has a very low input capacitance both in its on and in its off state. This is proved by fig 7E which shows the slope of Q-Vgs which is inversely proportional, in the first approximation to the input capacitance. In particular, from the cited figure the slope of the curve can be extrapolated before the so called Miller Plateau, when the device is still in its off state and after the Miller Plateau when the Vgs is above the threshold voltage and an inversion layer has formed in the channel region, i.e. when the device is in its on state. From these data a ratio Ciss-on/Ciss can be extrapolated. The dashed line indicates ideal behavior, it is preferred that the device

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adhere to ideal behavior as closely as possibly in order to minimize power loss (column 5 lines 1-10).

5. Further, the limitation must distinguish from the prior art in terms of structure rather than function, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971). Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Danly*, 263 F. 2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F. 2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

6. Regarding claim 2.

7. Williams teaches the device comprises a power MOSFET (fig 7a) (column 8 lines 15-25).

8. Regarding claim 3.

9. Williams teaches the behavior as shown by the dashed line (fig 7E) has a ratio of less than 1.5.

10. Regarding claim 4.

11. Williams teaches the behavior as shown by the dashed line (fig 7E) has a ratio of less than 1.

12. Regarding claim 5.

13. Williams teaches the device comprises a capacitor connected between the gate terminal and the gate of the device (fig 7H).

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14. Regarding claim 6.

15. The MOSFET has a vertical structure in that the gate and the source of the device are on one face of the chip body and the device and the drain of the of the MOSFET is provided on the opposite face of the chip body (fig 6c-6e).

16. Regarding claim 7.

17. Williams teaches the capacitor is integrated on the chip body (fig 7G, 7H).

18. Regarding claim 8.

19. Williams teaches The device comprises a capacitor, said capacitor is superimposed on the gate of the MOSFET (fig 7G, 7H).

20. Regarding claim 10.

21. Williams teaches that the gate is connected to a fourth terminal of the device (fig 6C).

22. The applicant does not specify the location or relation of the fourth terminal as opposed to any other terminal. Therefore the broadest reasonable interpretation of a forth terminal is that it may comprise the source or drain terminals as illustrated in figure 6c).

23.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

25. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US 6,291,298) as applied to claim 5 above and further in view of Jones (US 4,683,387).

26. Williams teaches elements of the claimed invention above. Williams does not teach that the capacitor is a discrete element.

27. Jones teaches that a discrete gate to source capacitor may be included (column 2 lines 25-35).

28. It would have been obvious to one of ordinary skill in the art to incorporate a discrete capacitor between the gate and a gate terminal in order to reduce the Miller effect thereby reducing the power loss and improving the device frequency.

29. Regarding claim 11.

30. Williams teaches The device package further comprises a bias (fig 6D). Said bias is supplied along conductive paths (fig 6D) all conductive paths provide a resistance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Goodwin whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJG

Andy Myers
Primary Examiner